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GNRFET BASED 8-BIT ALU

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ABSTRACT

The advancement in IC technology rendering area optimized and fast ICs is primarily attributed to MOSFET scaling theory. The scaling theory sustained the Moore's law till the channel size reached the nano-meter regime. The issues in MOSFET due to scaling aggregated and resulted in leakage currents and high power dissipation making the transistor unreliable. The research has been done to find a potential replacement for traditional CMOS and to sustain Moore's law. Many alternatives like

CNTFET and FINFET based designs were found, but Graphene Nano Ribbon (GNRFET) based design was found to be more viable option in terms of area and power dissipation. Thus analysis of the circuits built using GNRFET is necessary to demonstrate its merits. The paper describes the design of GNRFET based 8-bit ALU and its comparison with conventional CMOS design with respect to power consumption, showing 0.1589μW for GNRFET based design and 15.57μW for CMOS design. For the design, 10nm process technology was used for GNRFET and conventional CMOS designs.

KEYWORDS: CMOS, GNRFET ALU, Power Dissipation

1. INTRODUCTION

The advent of silicon MOSFET in 1960[1] led to tremendous advancement in VLSI chips. With the invention of silicon-CMOS, in 1965 Dr. Gordon Moore from Fairchild Semiconductor predicted that the number of transistors in a chip doubles every 18 months [2]. The reason for the success of Moore's law lies in reduction of the size of individual transistors according to the scaling theory. The sections 1.1 to 1.5 provide the literature review and the problem definition on theoretical grounds. Section 2 provides the work done and Section 3 and 4 provide the results obtained and conclusion respectively.

1.1 CMOS Scaling Theory

The reduction in chip size and development of ICs with huge number of transistors is attributed to the constant field scaling theory by Dr. Robert Dennard in 1974[3]. According to the constant field scaling theory- "If the device dimensions width-***W***, channel length-***L*** and oxide-thickness-***tox*** and voltages ***Vdd*** and threshold voltage-***Vth*** are scaled down by factor of 'a', with increased doping concentration by 'a'>1,all electric fields in the scaled transistor remain the same as in the original"[3]. The scaling theory thus provides the way to reduce the size of the transistor without affecting the functionality of the device. For a scaling factor of sqrt(2), the number of transistors per unit area doubles[4].

The scaling theory was responsible for channel size reduction in the silicon CMOS and technology advancement

from μm to nm range. As the VLSI technology entered the nano-meter regime, the MOSFET developed some issues as discussed in 1.2. The issues with silicon CMOS as the channel length is reduced are known as short-channel effects. The short channel effect arises due to scaling of MOS.

1.1 CMOS Scaling Issues

The scaling of CMOS no doubt reduces the size of the transistor, but also results in adverse effects on the functionality of the transistor. The scaling issues in MOS are:

- Sub-threshold conduction, threshold voltage (***Vth***) variation, carrier mobility degradation and Hot carrier effects in the **channel**[5]
- Direct gate tunnelling leakage current and gate depletion at the **gate** terminal[5]
- Parasitic resistance and parasitic capacitance on the **drain** and **source** terminals[5]
- Reverse biased junction leakage current in the **substrate**[5]

Among the above mentioned effects, the ones caused in channel are predominant and lead to leakage current and higher power dissipation. The increase in leakage current results in higher power dissipation and leads to unreliable device performance.

As the technology reaches sub-10nm [6], leakage current becomes a major limitation and thus a trade-off arises between area and Power dissipated. Thus below 10nm scaling theory cannot sustain Moore's law. This trade-off paves way for new material used in FETs to fabricate reliable devices and also maintain Moore's law. These materials include Fin-shaped FET (FinFET), Carbon Nano-tube FET (CNTFET) and Graphene Nano-Ribbon FET (GNRFET), among these Graphene has proven to be a potential replacement for conventional CMOS technology in terms of lower power consumption and faster operation.

1.3 Graphene

Graphene is a two dimensional sheet of Carbon atoms having a 2D honeycomb lattice. Graphene is intrinsically having zero band-gap between the valence-band and conduction-band making Graphene, a conducting material [7]. Thus intrinsic Graphene cannot be used as a material in FETs as FETs demand semiconducting material. Graphene is categorized into monolayer, bilayer or multilayer Graphene. The band-gap can be induced in bilayer Graphene to make it semi-conducting. The unbounded edges in the 2D sheet are passivated by various absorbents like hydroxyl group, carboxyl group, hydrogen, oxygen and ammonia [8]. To use Graphene in FETs, its band gap needs to be opened to make it a semiconductor. The attractive feature of Graphene is its high carrier mobility which renders faster switching times.

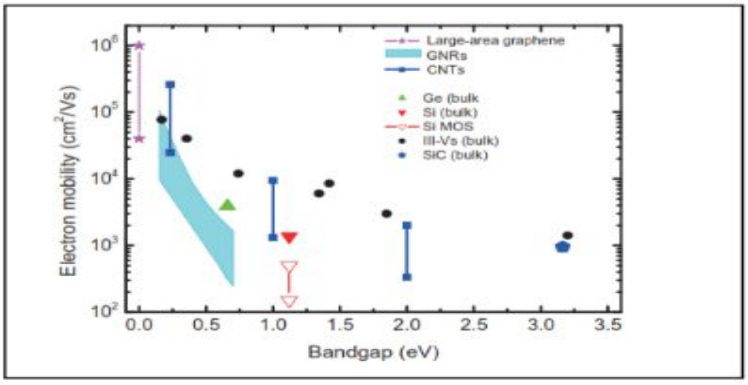

Figure 1: Electron Mobility Vs. Band Gap for Different Materials

1.4 GNRFET

The 2D Graphene sheets are patterned to 1D narrow strips or ribbons to open the band-gap. These 1D ribbons are called Graphene Nano Ribbon (GNR) and is semiconducting in nature owing to the fact that the band gap is inversely proportional to the width of the ribbon [9]. GNRs are long Graphene sheet with considerably lower widths, so that the carriers have only the lateral direction for movement. This carrier confinement in one direction gives rise to sub-bands with in-between gaps, thus making GNRs semiconducting. The number of dimmer lines determine the width of GNRFET. Another factor which determines the band-gap of the GNR is the chirality. On the basis of Chirality, GNRs can be further subdivided into Arm-chair GNR (AGNR) and Zig-zag GNR (ZGNR) [10].

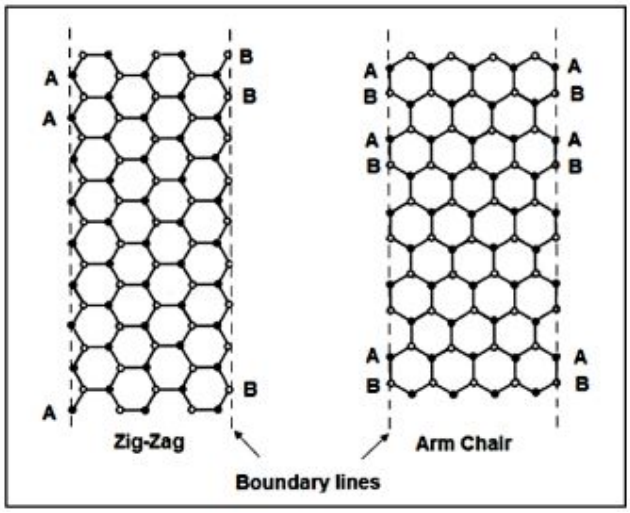

Figure 2: Lattice Structure of AGNR and ZGNR

The variations of GNR are due to their respective lattice structures. ZGNR possess a zigzag fashion of arrangement of Carbon atoms at the end of the lattice, whereas AGNR possess an edge that resembles an arm-chair in the lattice. AGNR band gap is finite and hence AGNR is semiconducting in nature. On the contrary, in ZGNR the band-gap is very small rendering metallic nature to ZGNR. Hence ZGNR finds minimal usage in FETs.

The fabrication of MOS-GNRFET can be accomplished by various methods like chemical synthesis [11], lithography [12], or unzipping from carbon nanotubes. GNR's of sub-10nm widths were manufactured and showed excellent

behaviour with respect to power and area [13]. The technique to integrate GNRs with existing Si-CMOS fabrication technology saves the cost of rebuilding the Silicon Foundries [14].The circuit design uses SPICE compatible GNRFET model [15].

1.5 Arithmetic Logic Unit (ALU)

The ALU is the basic computing unit of any CPU. The ALU consists of a parallel adder unit to perform arithmetic operations. The logical operations like NAND, NOR, XOR, XNOR are performed using the respective gate circuits. The operation to be performed depend on the selection lines from the control unit.

The parallel adder forms the critical path of the ALU and the choice of the type of parallel adder plays an important role in the performance of the ALU. The various types of Parallel adder structures and their merits and demerits are discussed here:

- Ripple Carry Adder (RCA): Carry-out of one stage forms the Carry-in of the next stage. Simple circuit and Low power dissipation are the advantages, whereas huge delay which is also proportional to the number of bits is the major disadvantage
- Carry Look Ahead adder (CLA): The Carry of all the stages are determined once the inputs arrive. Thus the delay is independent of the number of bits. It requires extra level of hardware to compute sum-bit, so complexity increase with number of bits
- Carry-Skip adder (CSA): A clever use of a skip-sub module makes the Cin appear at Cout apparently skipping the full-adder units. The CSA provides a delay of 3.022ns [16] compared to CLA with delay of 3.1ns [16], but requires less chip area and consumes less power [16].

The 4-bit RCA provides a delay of 1.55ns [17] and power dissipated is 0.763mW [17], whereas the 4-bit CLA provides a delay of 1.49ns [17] and power dissipated is 1.5mW [17]. Since Power is a major design concern, the proposed ALU uses RCA as its parallel adder structure.

The basic unit of parallel adder is the 1-bit Full-adder. The 28 transistors circuit is used to build the 1-bit Full-adder using complementary CMOS logic [18].

2. WORK DONE

An 8 bit arithmetic logic unit (ALU) consisting of three stages, namely, arithmetic block, logical block and operation selection block was designed.

The arithmetic block consists of adders and 4:1 multiplexers designed to perform increment, addition, 2's complement subtraction and buffering operations. 4:1 multiplexers are used to select one of the four arithmetic operations. 4:1 multiplexers are designed using NAND gates. Adders are used to perform arithmetic operations.

The logical block consists of 4:1 multiplexers and logical gates designed to perform NOT, NAND, NOR and XOR operations designed using NAND gates. 4:1 multiplexers are used for selection of one of the four operations.

The operation selection block consists of 2:1 Mux designed using NAND gates. This block is used for selection of either arithmetic or logical operations.

The schematic of the ALU is as shown in the figure 3.

The proposed ALU performs the following functions:

Arithmetic operations: Addition, carry addition 1's complement subtraction, 2's complement subtraction, increment, decrement and buffering operation

Logical operations: NOT, NAND, NOR, XOR The proposed ALU consists of the following circuits

Table 1: ALU Component List

Circuit	Number Used
1-bit Full-adder	8
4x1 MUX	16
2x1 MUX	8

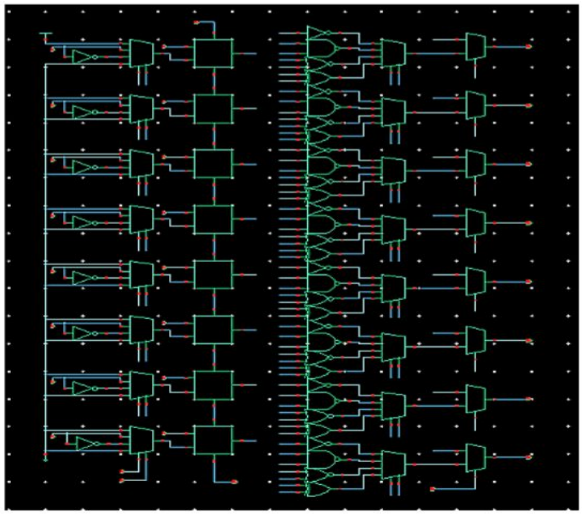

Figure 3: Schematic of the Proposed ALU

The operation that needs to be performed depends on the three selection lines (s2, s1, s0) from the control unit. The dependence on the control lines is shown below:

Table 2: ALU Operations List

S2	S1	S0	Operation performed
0	0	0	A+1
0	0	1	A+B
0	1	0	A+B'
0	1	1	A+0
1	0	0	A'
1	0	1	(A&B)'
1	1	0	(A|B)'
1	1	1	A XOR B

3. RESULTS

The proposed ALU has been simulated in Hspice tool for both the technologies. For GNRFET technology, the channel width chosen is 10nm and the number of nanoribbons chosen is 6 with the number of dimer lines being 12. For CMOS technology, the channel width is 10nm.

The circuits have been simulated to find performance parameters like the total power dissipation and the critical propagation delay. The results thus obtained have been tabulated (Table 3) and interpreted graphically (Figure 4).

Table 3: Power Consumption

Technology	Power(μW)	Worst-case Delay(ps)
CMOS	15.57	95.56
GNRFET	0.1589	33.97

The low power consumption in case of GNRFET is due to low gate capacitance, tunnelling current and low VDD. Since power delay product is an important performance parameter, the optimum VDD was found by plotting VDD vs power delay product (Figure 5) for 2x1 MUX.

From the VDD vs Power consumption graph (Figure 5a) it can be noted that, power consumption increases exponentially when VDD is above 0.7 and decreases when VDD is less than 0.7V. On the other hand, delay (Figure 6b) is found to be maximum when VDD is 0.3V and gradually reduces on either side of 0.3V point. From these results it has been found that power and delay value are optimal when VDD is around 0.5V.

Power Consumption Comparison

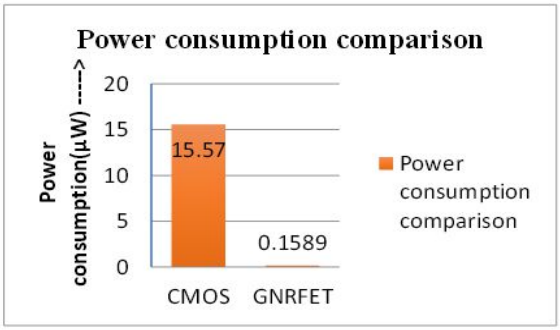

Figure 4: Graph of Power Consumption

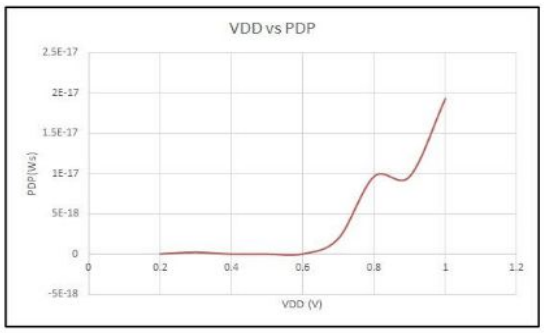

Figure 5: VDD vs. Power Delay Product of 2x1 MUX

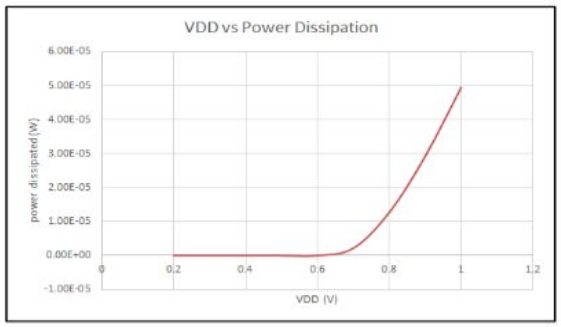

Figure 5a: VDD vs. Power Consumption of 2x1 MUX

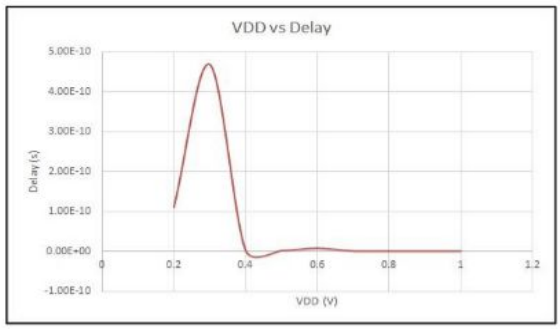

Figure 5b: VDD vs. Delay of 2x1 MUX

CONCLUSIONS

Due to the importance of the ALU, a lo w voltage and low power GNRFET based ALU has been designed and its performance parameters have been compared with that of CMOS design.

As the simulation results illustrated, there was substantial improvement in the performance parameter of GNRFET based design over CMOS design. Moreover GNRFET can be scaled down to 2nm technology and hence can sustain Moore's law for next 2 to 3 years

Future Work

The design can be improved with modifications in future studies. Further improvement can be achieved by utilizing various adder topologies. Optimization of power-delay product is required to incorporate this design in processors.

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Bangalore, in 1995 and Ph.D in VLSI Design area from Vsvesvaraya technological University. He has three Text books with McGraw-Hill (TMH) and Pearson Education, 4 International & 8 National papers to his credit. He has successfully guided many Post-graduate and Undergraduate projects. He is a life member in Indian Society for Technical Education (ISTE) and Institution of Electronics and Telecommunication Engineers (IETE). His research interests include the areas of VLSI design, Microprocessor and Microcontroller based system designs, Embedded system design, SOC design and Computer networking.

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